CLAIMS

1. A thin film transistor (100) on a substrate (102) comprising:

a semiconductor layer (120) having a first doped region (121) and a second doped region (122) in between a first further doped region (125) and a second further doped region (126), and having an undoped region (123) in between the first doped region (121) and the second doped region (122), the first doped region (121) and the second doped region (122) having a lower conductivity than the first further doped region (125) and the second further doped region (126); and

an oxide layer (140) partially covering a surface of the semiconductor layer (120), the oxide layer (140) carrying:

- a conductive gate (104) over the undoped region (123) having a first side and a second side substantially perpendicular to the oxide layer (140);
- a first spacer (111) and a second spacer (112) adjacent to the first side and second side of the conductive gate (104) respectively;
- a first insulating spacer (115) adjacent to a side of the first spacer (111) opposite the first side of the conductive gate (104); and
- a second insulating spacer (116) adjacent to a side of the second spacer (112) opposite the second side of the conductive gate (104);

the thin film transistor (100) further comprising:

a first conductive contact (135) with the first further doped region (125); and

a second conductive contact (136) with the second further doped region (126).

2. A thin film transistor (100) as claimed in claim 1, wherein the first spacer (111) and the second spacer (112) comprise a conductive material.

3. A thin film transistor (100) as claimed in claim 1 or 2, wherein the first conductive contact (135) and the second conductive contact (136) comprise a silicide layer.

4. A thin film transistor (100) as claimed in claim 1 or 2, wherein the semiconductor layer (120) comprises a polycrystalline silicon material.

5. A method for producing a thin film transistor (100) on a substrate comprising a semiconductor layer (120) having an undoped region (123) in between a first doped region (121) and a second doped region (122) and an oxide layer (140) partially covering a surface of the semiconductor layer (120), the oxide layer (140) carrying a conductive gate (104) over the undoped region (123), the conductive gate (104) having a first side and a second side substantially perpendicular to the oxide layer (140); the first doped region (121) and the second doped region (122) having been formed in a self-alignment step using the conductive gate (104) as a mask, the method comprising the steps of:

providing a first spacer (111) and a second spacer (112) on the oxide layer (140) adjacent to the first side and second side of the conductive gate (104) respectively;

implanting a first further doped region (125) and a second further doped region (126) into the semiconductor layer using the conductive gate (104), the first spacer (111) and the second spacer (112) as a further mask, the first further doped region (125) and the second further doped region (126) being more conductive than the first doped region (121) and the second doped region (122);

providing a first insulating spacer (115) on the oxide layer (140) adjacent to the first spacer (111) opposite the first side of the conductive gate (104) and a second insulating spacer (116) on the oxide layer (140) adjacent to the second spacer (112) opposite the second side of the conductive gate (104);

removing an exposed area of the oxide layer (140) covering the first further doped region (125) and the second further doped region (126); and

providing the first further doped region (125) with a first conductive contact (135) and the second further doped region (126) with a second conductive contact (136).

6. A method as claimed in claim 5, wherein the step of providing a first spacer (111) and a second spacer (112) comprises depositing a conductive spacer material.

7. A method as claimed in claim 5 or 6, wherein the step of providing the first further doped region (125) with a first conductive contact (135) and the second further doped region (126) with a second conductive contact (136) comprises reacting a conductive material with the semiconductor layer (120) to form a silicide.

8. A method as claimed in claim 5 or 6, wherein the step of removing an exposed area of the oxide layer (140) covering the first further doped region (125) and the second further doped region (126) is performed using the conductive gate (104), the first spacer (111), the second spacer (112), the first insulating spacer (115) and the second insulating spacer (116) as a mask.

9. An electronic device (200) comprising an active matrix array (220) coupled to a first driver circuit arrangement (240) and a second driver circuit arrangement (260), the first driver circuit arrangement (240) and the second driver circuit arrangement (260) being coupled to a power supply (280), at least one of the matrix array (220), the first driver circuit arrangement (240) and the second driver circuit arrangement (260) comprising a plurality of thin film transistors (100) as claimed in any of the claims 1-4.

10. An electronic device (200) as claimed in claim 9, wherein the power supply (280) comprises battery means.

11. A thin film transistor (100) substantially as described herein with reference to the drawings.

12. A method for producing a thin film transistor (100) substantially as described herein with reference to the drawings.

13. An electronic device (200) substantially as described herein with reference to the drawings.